REMARKS

Applicants respectfully request reconsideration of the prior art rejections set forth by the Examiner under 35 U.S.C. sections 102 and 103. Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicants' presently claimed invention.

More specifically, Applicants presently claimed invention is directed to a pseudo-wafer structure wherein known good die are incorporated into a common structure or wafer wherein the known good die are encapsulated with a resin material to form the pseudo-wafer which is amenable to subsequent processing for forming electrodes and the like. Advantageously, by forming the pseudo-wafer for the formation of electrodes, substantial economic advantage is achieved because the required solder bumps are not formed on the electrodes of defective products. Batch processing of known good die can be advantageously achieved. The prior art references of record provide no teaching or suggest whatsoever regarding this advance in the art.

In contrast with the presently claimed invention, the prior art Camien reference merely describes an innovation directed to providing stackable integrated circuit chips or die layers which permit chips having different functions and different physical areas to be stacked as if they were the same size chips using stacking and electrical connection techniques and tools which have been developed for same size chips. As described in this reference, prior to stacking, one or more known good a die chips are used to create the wafer by locating those known good die chips in a potting fixture. Potting material is flowed into the fixture which is enclosed and the potting material is cured. The resulting neo-wafer is removed from the fixture

and is subjected to a pre-stacking process. There is no teaching or suggest whatsoever regarding the batch processing and formation of solder bump electrodes, for example as described in the instant application. The Examiner merely makes the conclusory assertion that it would have been obvious to perform batch processing on a pseudo-wafer.

Significantly, neither Camien nor the combined teaching of this reference with the Wollf VLSI publication teach or suggest the claimed subject matter. It is important to recognize that the purported combination of references does not result in the claimed subject matter. This is because Camien merely describes the formation of stackable integrated circuit chip layers and the reference does not teach or suggest the formation of a pseudo–wafer's for the limited purpose of batch processing the individual chips so that it is not necessary to form solder bumps on defective chips.

Camien only teaches that layer structures comprised of different chips to be electronically interconnected may be provided. Significantly, however, this does not provide the requisite teaching or suggestion regarding batch processing and like of only known good die.

The remaining rejections based upon the Paik reference are similarly defective because this reference merely describes the use of wafer strips which are not known good die as required by the claims in the instant application.

Accordingly, in light of the foregoing, Applicant submits that all claims now stand in condition for allowance because the prior art references cited by the examiner failed to teach or suggest the presently claimed subject matter.

Respectfully submitted,

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